

Customer No.: 31561  
Application No.: 10/709,372  
Docket NO.: 12409-US-PA

**REMARKS****Present Status of the Application**

The Office Action objected to the specification because of incorrect reference sign. The Office Action rejected claims 1-10 under 35 U.S.C. 102(e), as being anticipated by Chang et al. (U.S. 6,486,028; hereafter Chang). The Office Action also rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes). Applicants have amended the specification to overcome the objection and have amended claims 1 and 9 to improve clarity. After entry of the foregoing amendments, claims 1-10 remain pending in the present application, and reconsideration of those claims is respectfully requested.

**Summary of Applicants' Invention**

The Applicants' invention is directed to a non-volatile memory cell with a gate, a first source/drain region, a second source/drain region and a third source/drain region. The gate is located in a trench within a substrate, the first source/drain region (206) is located in the substrate under the bottom of the gate, the second source/drain region is located at one side of the gate in the substrate and the third source/drain region is located at the other side of the gate in the substrate. Since the second source/drain region and the third source/drain region are electrically connected to a common bit line, the non-volatile memory cell can be regarded as two transistors connected in parallel. In this structure, the gates of the transistors are electrically connected to a common word line, the sources are

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electrically connected to a common source line and the drains are electrically connected to a common bit line (as shown in Fig. 3 and paragraph [0036]). Hence, with this configuration, the density of current flowing through the non-volatile memory cell is increased and the efficiency of programming/erasing operation is improved.

#### Discussion of Office Action Objections

According to the Office Action, the specification is objected to because of the incorrect reference sign. In response thereto, Applicants have amended the reference number 201 to 210 in the paragraph [0031]. No new matter has been added into the application by the amendment made herein.

#### Discussion of Office Action Rejections

*The Office Action rejected claims 1-10 under 35 U.S.C. 102(e), as being anticipated by Chang et al. (U.S. 6,486,028; hereafter Chang) and asserted that Chang discloses all claimed features of the present invention.*

Applicants respectfully traverse the rejections for at least the reasons set forth below.

It is well established that anticipation under 35 U.S.C. 102 requires each and every elements of the rejected claims must be disclosed exactly by a single prior art reference.

The amended independent claim 1 is allowable for at least the reason that Chang fails to teach or disclose each and every features of the proposed amended independent

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claim 1. AS amended, claim 1 recites:

Claim 1. A non-volatile memory cell, comprising:  
a substrate, having a trench thereon;  
a gate, formed within the trench;  
a first source/drain region, formed at a bottom of the trench;  
a composite dielectric layer, formed between the gate and a surface of the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer;  
a second source/drain region, formed in the substrate on one side of the gate; and  
a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line.

*(Emphasis added).* Applicants submit that claim 1 patently defines over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

In the present invention, the second source/drain region located at one side of the gate 208 (as shown in 2B) and the third source/drain region located at the other side of the gate 208 are electrically connected to a common bit line in order to increase the density of the current flowing through the non-volatile memory cell so as to improve the efficiency of programming/erasing operation (as shown in Fig. 3 and paragraph [0036]).

However, Chang fails to teach or suggest that the first source/drain region 104 and the second source/drain region 106 (as shown in Fig. 6 in the cited art) are electrically connected to a common bit line. There is no evidence founded in the cited art to support that Chang intend to increase the density of current flowing through the non-volatile memory cell. Hence, there is no motivation for skilled artisan, who wants to increase the current density, to modify Chang's application by re-designing the connecting relationship between the first source/drain region 104 and the second source/drain region

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106.

Therefore, Chang substantially fails to teach each and every feature of claim 1 and therefore, Chang cannot possibly anticipate the claimed invention as claimed in the proposed independent claims1 in this regard.

Claims 2-9, which depend from claim 1, are also patentable over Chang, at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1-10 patently define over Chang, and therefore should be allowed. Reconsideration and withdrawal of the above rejections is respectfully requested.

*The Office Action also rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes).*

Since claims 7 and 8 are dependent claims which further define the invention recited in claim 1, Applicants respectfully assert that these claims also are in condition for allowance according to the same reasons as discussed above for the rejection 102. Thus, reconsideration and withdrawal of this rejection are respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office  
7<sup>th</sup> Floor-1, No. 100  
Roosevelt Road, Section 2  
Taipei, 100  
Taiwan  
Tel: 011-886-2-2369-2800  
Fax: 011-886-2-2369-7233  
Email: [belinda@jcipgroup.com.tw](mailto:belinda@jcipgroup.com.tw)  
[Usa@jcipgroup.com.tw](mailto:Usa@jcipgroup.com.tw)

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